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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PHU, PHUONG M

ART UNIT

PAPER NUMBER

2631

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18

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/887,481	POSTI, HARRI
	Examiner	Art Unit
	Phuong Phu	2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-38 and 40-49 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-38, 40-49 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____
4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 3/17/04.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 23-38, 40-43, 46-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites the limitation “said input different digital signals” on line 14. This limitation is lack of antecedent basis. The limitation is suggested to be changed to --“said different digital signals-- in order to be consistent with “different digital signals” on line 2.

Similarly, “said different digital signals”, on line 14 of claim 46, 47 and 49, and on line 16 of claim 48, are lack of antecedent basis.

Claim 33 recites the limitation “the composite signal” on line 2. This limitation is lack of antecedent basis.

Claims, (if any) depended on above claims, are therefore also rejected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 23-25, 28-31, 33, 37, 38, 40, 42-45, 47 and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Carney et al (5,937,011), prior art of record.

As per claims 23, 44, 45, 47 and 48, see figure 1 and col. 2, line 20 to col. 4, line 17, Carney et al discloses a method and associated system comprising:

input step/means (inherently included) for receiving a plurality of different digital signals (121-1,..., 121-n);

modulator step/means (120) for modulating said different digital signals at respective carrier frequencies;

combiner step/means (122) for combining said plurality of different digital signals to provide a composite digital signal (15);

D/A converting step/means (160) for converting said composite signal into a composite analog signal;

amplifier step/means (including (18)) for receiving and amplifying said composite analog signal;

predistortion step/means (14) for predistorting said plurality of different digital signals wherein the predistortion performed by step/means (14) is performed after the modulator step/means and prior to the amplifier step/means, and dependent on a difference between input signals in a signal (125) (which comprises a version of said different digital signals) and the output of said amplifier step/means.

As per claim 24, Carney et al discloses that said input step/means separately receives each of said different digital signals (see figure 1).

As per claim 25, Carney et al discloses a combiner means (122) to provide a composite digital signal (see figure 1).

As per claim 28, Carney et al discloses that said predistortion step/means predistorts the composite digital signal (see figure 1).

As per claim 29, Carney et al discloses a feedback path (165, 166) (see figure 1).

As per claims 30 and 33, Carney et al discloses that the distortion step/means compares the output from the amplifier step/means for the feedback path with the signals received by the input step/means and provides predistortion values applied to a subsequent signal received by the input step/means (see figures 1 and 2A, and col. 4, lines 18-52).

As per claim 31, Carney et al discloses means (23, 165, 166) for separating the output of the amplifier step/means into a signal (150) comprising a plurality of different digital signals.

As per claim 37, Carney et al discloses that the amplifier step/means comprises an amplifier (18).

As per claim 38, Carney et al discloses that said predistortion step/means compensates for the nonlinearity of amplitude of the amplifier (see col. 4, line 49-52).

As per claim 40, Carney et al discloses an A/D converter step/means (166) as claimed (see figure 1).

As per claims 42 and 43, Carney et al discloses a station comprising the method and associated system (see col. 2, line 20-35).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 23-27, 29-38 and 40-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helms (2001/0014592), prior art of record, in view of Carney et al.

As per claims 23 and 44-49, see figure 4 and page 2, section [0028] to page 3, section [0035], Helms discloses a method and associated system comprising:

combiner step/means (DUC, SUM) for combining a plurality of different carrier-related signals (in₁,...,in_n) to provide a composite digital signal (in_{pr});

D/A converting step/means (DAC) for converting said composite digital signal into a composite analog signal;

amplifier step/means (UM, PA) for receiving and amplifying said composite analog signal;

predistortion step/means (PDD) for predistorting said plurality of different carrier-related signals wherein the predistortion performed by step/means (PDD) is performed prior to the amplifier step/means, and dependent on the difference between said different carrier-related signals (in₁,..., in₂) and the output (out_m) of said amplifier step/means.

Further regarding to claims 46 and 49, Helms further discloses an A/D converter step/means (DM, ADC) for converting the output of the amplifier step/means into a composite digital signal comprising a plurality of digital signals outputted from means (ADC); and a channelizing step/means (DDC) for converting said composite digital signal into a plurality of different digital signals (see figure 4).

Helms does not disclose input step/means for receiving a plurality of different digital signals and modulating step/means for modulating said different digital signals at respective carrier frequencies. He neither discloses that predistortion step/means (PDD) is performed after a modulation.

However, he discloses that said plurality of different carrier-related signals ($in1, \dots, inn$) are formed by being located to respective carrier frequencies $1-n$ over a bandwidth (B) (see section [0028] and figure 2), but he does not disclose how said plurality of different carrier-related signals are formed in detail. On the other hand, Carney et al teaches that n different carrier-related signals allocated on respective carrier frequencies over a bandwidth are formed by modulating a plurality of n received data digital signals ($I21-1, \dots, I21-n$) by using a plurality of modulating step/means ($120-1, 120-n$) to allocate said n received data digital signals on respective carrier frequencies equal spaced apart over a frequency bandwidth (see col. 3, lines 26-33 and lines 38-43). Therefore, for an application, it would have been obvious for one skilled in the art, when building Helms invention, to form said plurality of different carrier-related signals ($in1, \dots, inn$) by using a plurality of modulating step/means, as taught by Carney et al, to allocate n received different digital signals on respective carrier frequencies equal spaced apart over the required frequency bandwidth (B). As a result, the implementation of Helms in view of Carney et al, discloses modulating step/means for modulating different digital signals at respective carrier frequencies to form said different carrier-related signals ($in1, \dots, inn$), as a plurality of different carrier modulated signals, and said predistortion step/means (PDD) being performed after the modulation of said plurality of modulating step/means wherein an input means is inherently included for receiving said different digital signals.

As per claim 24, in Helms in view of Carney et al, said modulating step/means inherently separately receives each of said different digital signals in order to perform a modulation with each of them with a corresponding carrier in order to provide separate carrier modulated signals (in_1, \dots, in_n) at the input of means (PDD) (see Helms, figure 4).

As per claim 25, Helms discloses a combiner means (DUC, SUM) to provide a composite digital signal (see figure 4).

As per claim 26, Helms discloses said distortion step/means, using means (PD₁, ..., PD_n), predistorts individually said each of said plurality of different carrier modulated signals (see figure 4).

As per claim 27, Helms discloses said distortion step/means predistorts said plurality of different carrier modulated signals before being combined in said combiner step/means (see figure 4).

As per claim 29, Helms discloses a feedback path (DDC, ADC, DM) (see figure 4).

As per claims 30 and 33, Helms discloses that the distortion step/means compares the output from the amplifier step/means for the feedback path with the signals received by the input receiving and modulating step/means and provides predistortion values applied to a subsequent signal received by the input receiving and modulating step/means (see figure 4 and page 2, section [0029] to page 3, section [0033]).

As per claim 31, Helms discloses means (AK, DM, ADC) for separating the output of the amplifier step/means into a signal comprising a plurality of different digital signals ($out_{m1}, \dots, out_{mn}$) (see figure 4).

As per claim 32, Helms discloses that said predistortion step/means compares each of said separated signals with the corresponding signal received from said input receiving and modulating step/means to determine predistortion values to be altered (see figure 4 and page 2, section [0029] to page 3, section [0033]).

As per claim 34, Helms discloses that said predistortion step/means provides a plurality of predistortion values stored in means (LUT), each provided for the respective carrier frequency (see figure 4).

As per claim 35, Helms discloses that each of said predistortion values corresponding to a respective carrier frequency takes into account characteristics of other carrier frequencies (see page 1, section [0009]).

As per claim 36, Helms discloses that said characteristics comprise frequency and distortion (see page 1, section [0009]).

As per claim 37, Helms discloses that the amplifier step/means comprises an amplifier (PA).

As per claim 38, Helms discloses that said predistortion step/means compensates for the nonlinearity of amplitude of the amplifier (see page 1, section [0009]).

As per claims 40 and 41, Helms discloses an A/D converter step/means (ADC) as claimed (see figure 4).

As per claims 42 and 43, Helms discloses a station comprising the method and associated system (see pages 2, section [0024]).

Response to Arguments

8. Applicant's arguments filed on 3/17/04 have been fully considered but they are not, in part, persuasive.

Applicant's arguments with respect to the rejections, under 35 U.S.C., second paragraph, have been considered. The respective rejections to claims 44 and 45 are now withdrawn. However, claims 23-38, 40-43 and 46-49, after being amended, are still rejected, under U.S.C., second paragraph, with reasons set forth above.

Applicant's arguments with respect to the rejections, under 35 U.S.C, 102(e), to claims 23-27, 29-38 and 40-49, as being anticipated by Helms, have been considered but moot in view of a new ground of rejection as set forth above.

Applicant's arguments with respect to the rejections, under 35 U.S.C, 102(b), to claims 23-25, 28-31, 33, 37, 38, 40, 42-45, 47 and 48, as being anticipated by Carney et al, are not persuasive. The applicant mainly argues that with respect to independent claims 23 and 44, 45, 47 and 48, Carney et al does not disclose predistorting a plurality of different digital signals during or after modulation of said different digital signals and prior to amplification of a composite analog signal. The examiner respectfully disagrees. See figure 1, Carney et al discloses predistorting step/means (14) comprising means (140) which predistorts a combined signal being outputted from means (122) and received at port (A) of means (140) wherein said combined signal is a combination of plurality different digital signals outputted from modulation means (120-1,..., 120n), namely, said predistorting step/means (14) predistorts said plurality different digital signals (in form of said combined signal) after the modulation performed by means (120-1,..., 120n), as claimed. And further, see figure 1, Helms discloses predistorting

Art Unit: 2631

step/means (14) is performed prior to amplification (18) of a composite analog signal (15 or 17), as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 703-308-0158. The examiner can normally be reached on M-F (8:30-6:00) First Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuong Phu
Primary Examiner
Art Unit 2631

Phuong Phu
Phuong Phu
04/28/04

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